REMARKS

Claims 5-9 and 13-19 are all the claims pending in the application.

Claims 5 and 14 have been amended to further clarify the claimed invention.

PRIOR ART REJECTIONS

Claims 5-9 and 13-19 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Chakrovorty (U.S. Patent No. 6,181,569) in view of Qi (U.S. Patent No. 6,774,497) and/or in view of Lance (U.S. Patent No. 5,697,148) and/or Ho (U.S. Patent No. 6,849,955). Applicants traverse these rejections because the cited references fail to disclose or suggest all of the claim limitations. Specifically, at least the following limitations are not disclosed or suggested:

Claim 5:

a plurality of bond pads on an upper surface of integrated circuit chip, wherein each of said bond pads is aligned in ***only a central row***, and

a plurality of conductive bumps formed on the plurality of bond pads;

Claim 14:

a plurality of bond pads on an upper surface of integrated circuit chip, wherein each of said bond pads is aligned in ***only a plurality of central rows***, and

a plurality of conductive bumps formed on the plurality of bond pads;

As explained in Paragraph 9 of the patent specification, a problem associated with the individual mounting of a singulated IC chip onto a substrate is the difficulty of balancing the IC chip on a single, central row of bumps. The present claimed invention overcomes this problem by mounting an array of chips with center row(s) of bumps on a substrate so that balance can be

achieved. This also enables multiple chips to be handled and processed together, rather than individually, thereby making the process more efficient and less costly [paragraph 28].

Chakravorty describes providing first metal bumps on a wafer, depositing encapsulant over the metal bumps, polishing to expose top surface of the metal bumps. Second metal bumps are provided over the exposed first metal bumps and the wafer is singulated into individual chips. Chakravorty, however, does not disclose or suggest mounting the wafer or an array of integrated circuit chips with only a center row or rows of bumps on a substrate. The bumps are located over the entire surface of the substrate.

Likewise, Qi et al. discloses mounting a chip with bumps onto a substrate, but does not disclose mounting an array of chips with only a center row or rows of bumps on the substrate.

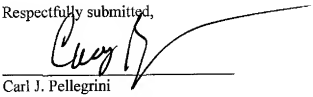
Neither Chakravorty or Qi et al. describe the problem of balancing a center row bumped chip onto a substrate. Nor do they disclose the advantageous technical effect of mounting an array of integrated circuit chips with center row bumps onto a substrate and processing them as multiple units. The skilled artisan, with knowledge of the cited prior art would therefore be unable to arrive at the present invention as defined by amended claim 5 due to the lack of guidance from these disclosures. It is therefore submitted that amended claims 5 and 14 and their dependent claims are inventive over the cited prior art.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the

Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



Carl J. Pellegrini
Registration No. 40,766

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860
WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Date: June 8, 2010